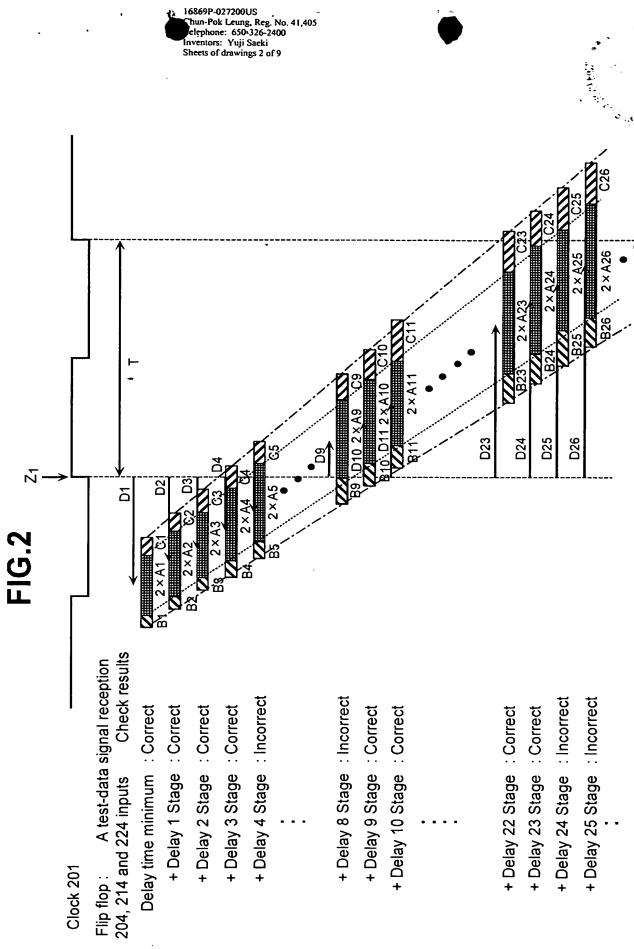
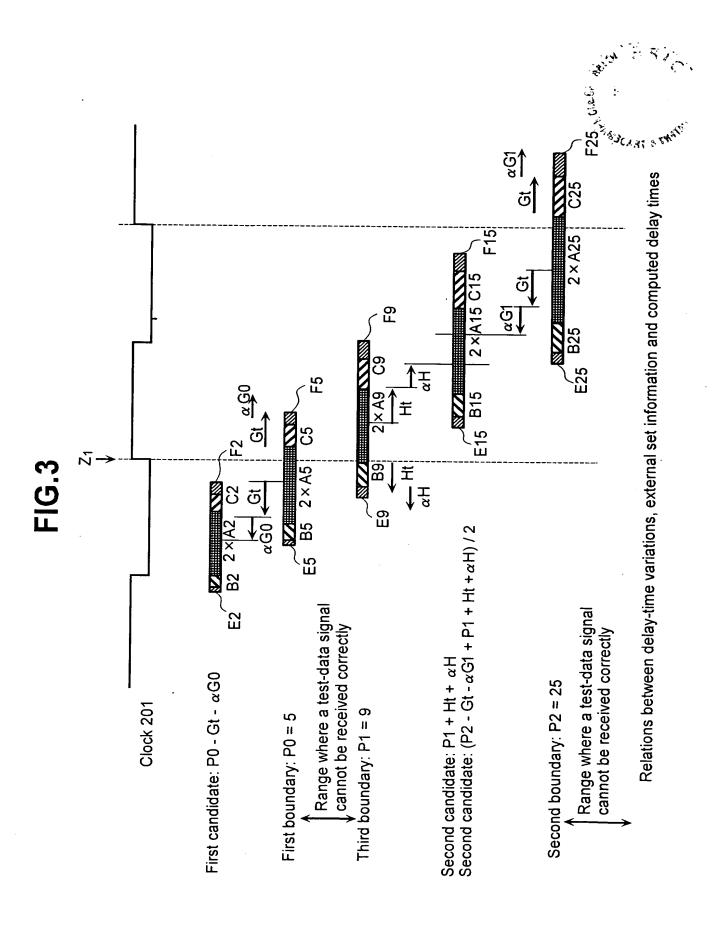
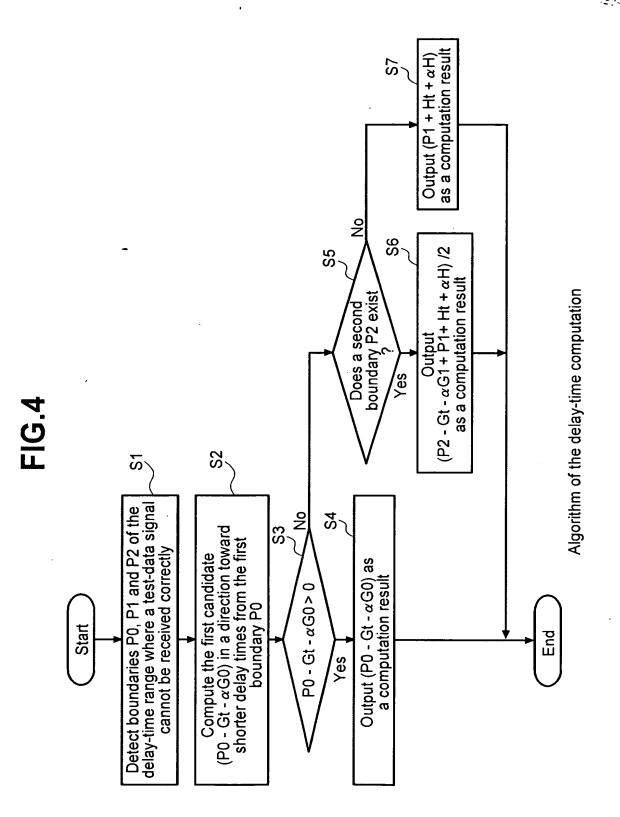


**FIG.1** 

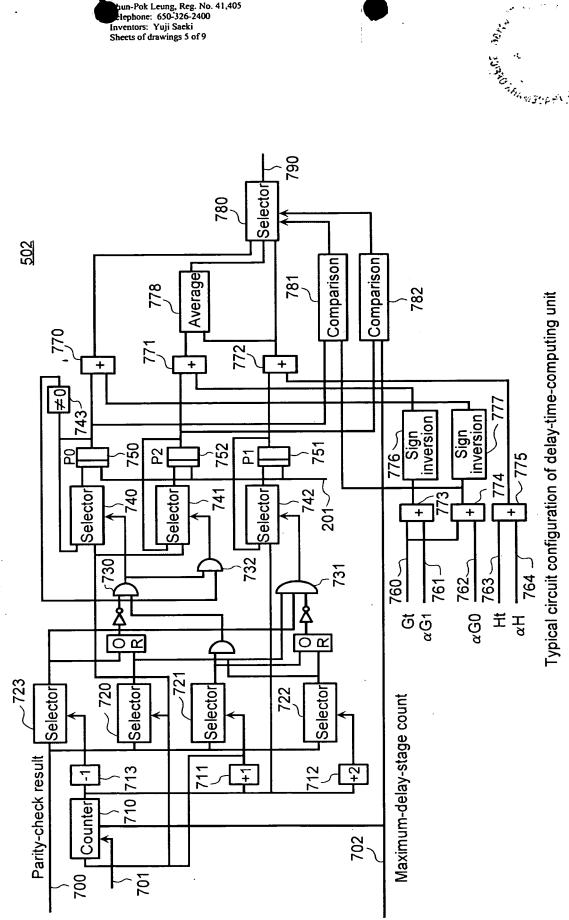


Phase relations between received-data indeterminate times and a clock signal

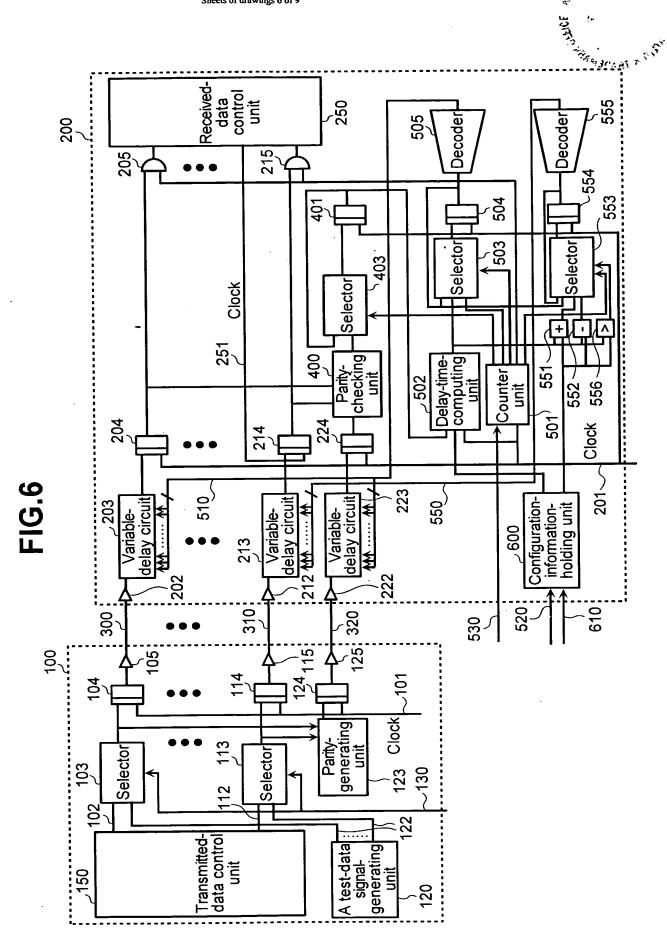




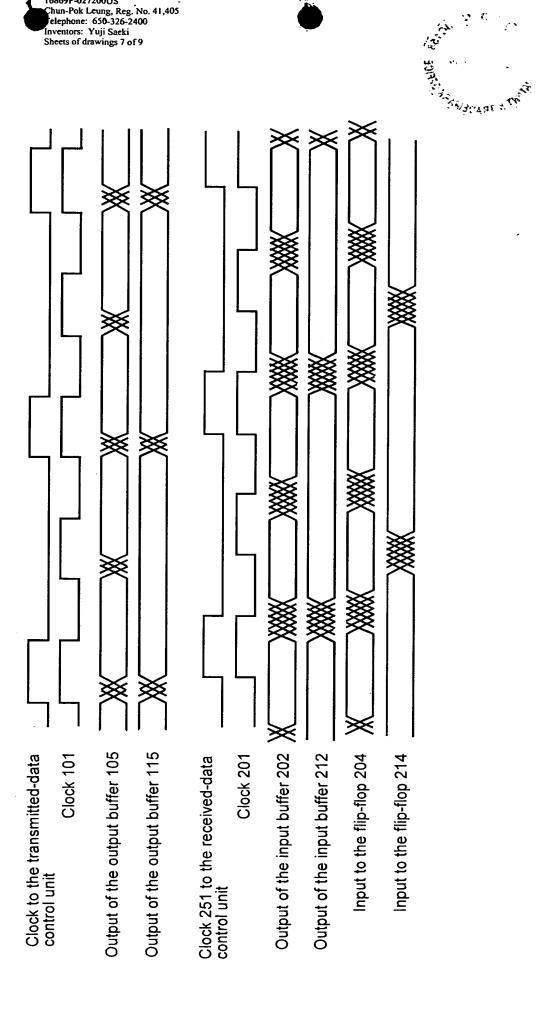


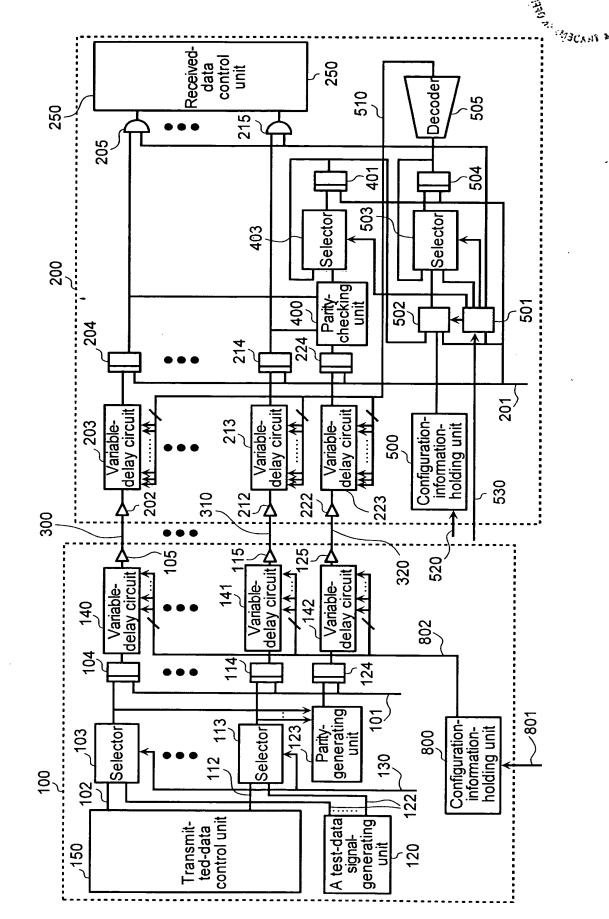


Typical circuit configuration of delay-time-computing unit



**FIG.7** 





**FIG.8** 

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Sheets of drawings 9 of 9

FIG.9

